

PRE-CONFERENCE TUTORIAL

27th Norchip Conference

15 November 2009 at 13.00-17.00, Trondheim, NORWAY



Norchip

Hybrid CMOS/Nanogrid Architectures and Circuits

Abstract

The goal of this 4-hour tutorial is to review the recent work on the development of hybrid digital semiconductor/nano-electronic integrated circuits. The nano-electronic circuits described here are primarily nanogrid (nano-crossbar) structures. These structures will most likely be fabricated on top of traditional CMOS technology, often in a hybrid architecture called CMOL. It is likely that such nanogrid technologies will be the first nanoelectronic technologies to be manufactured in volume and find wide-spread use. The basics of nanogrid techniques as well as some sample architectures and simulations will be presented, including terabit-scale memories, FPGA-like reconfigurable logic circuits, reconfigurable DSP-like circuits, and mixed-signal neuromorphic circuits.

In addition, the state of the art in nanogrid fabrication will be discussed, such as the recent experimental demonstration of reproducible crosspoint devices and nanowire crossbars with 15-nm-scale half-pitch. Much of this tutorial has been borrowed from "Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges," a tutorial offered by K. Likharev, D. Strukov, and G. Rose at ISCAS 2008, with the authors' permission.

Outline:

- 13.00 Introduction:
 - Critical review of the prospects offered by nanoelectronics
 - Introduction to nanogrids and hybrid CMOS/nano circuits
 - Hybrid circuit species, including CMOL, FPNI, and 3D CMOL
- 13.45 Digital hybrid circuit simulation and CAD:
 - Resistive memories, CMOL FPGA, Reconfigurable DSP
- 14.30 Mixed-signal circuit simulation:
 - Mixed-signal hybrid circuits, Neuromorphic networks
- 15.15 Coffee
- 15.35 Low-level development of hybrid circuits:
 - Nanoelectronic device modeling and fabrication
 - Circuit-level issues in hybrid CMOS/nano systems
 - Majority-logic and NDR device options for hybrid circuits
- 16.35 Prospects and challenges:
 - Hybrid circuit development roadmap
 - Hardware/fabrication challenges
 - Software/CAD challenges and most urgent research tasks

Selected publications:

- [1] Stan, M.R., et al., *Molecular Electronics: From Devices and Interconnect to Circuits and Architecture*. Proceedings of the IEEE, 2003. 91(11): p. 1940-1957.
- [2] Likharev, K.K. and D.B. Strukov, *Prospects of development of digital hybrid CMOS/nanoelectronic circuits*, in *Nanoarch 07*. 2007: San Jose, CA.
- [3] Likharev, K.K., *Hybrid semiconductor/nanoelectronic circuits: Freeing advanced lithography from the alignment accuracy burden*. J. Vac. Sci. Technol. B, 2007. 25(6)
- [4] Gao, C. and D. Hammerstrom, "Cortical models onto CMOL and CMOS - architectures and performance/price," *IEEE Tran. on Circuits and Systems-I*, vol. 54, pp. 2502-2515, Nov. 2007

Dan Hammerstrom received a BSEE degree from Montana State University, the MSEE degree from Stanford University, and the PhD EE degree from the University of Illinois at Urbana-Champaign. He was an Assistant Professor in the Electrical Engineering Department at Cornell University from 1977 to 1980. In 1980 he joined Intel in Oregon, where he participated in the development and implementation of the iAPX-432, the i960, and iWarp. He joined the faculty of the Computer Science and Engineering Department at the Oregon Graduate Institute in 1985 as an Associate Professor. In 1988 he founded Adaptive Solutions, Inc., which specialized in high performance silicon technology (the CNAPS chip set) for image processing and pattern recognition. He returned to the Oregon Graduate Institute in 1997, where he was the Doug Strain Professor in the Computer Science and Engineering Department until 2004.

He is now a Professor in the Electrical and Computer Engineering Department and Associate Dean in the Maseeh College of Engineering and Computer Science at Portland State University. Dr. Hammerstrom holds joint appointments in the Biomedical Engineering Division of the Oregon Health & Science University, and in the IDE (Information, Computation, and Electronics) Department at Halmstad University, Halmstad, Sweden. He has been an Associate Editor for the IEEE Transactions on Neural Networks, the Journal of the International Neural Network Society (INNS), and the International Journal of Neural Networks. He is currently an Associate Editor for the IEEE Transactions on Nanotechnology. He has authored over seventy research papers and eight book chapters, and holds seven patents. Dr. Hammerstrom has been a Visiting Scientist at the Royal Institute of Technology in Stockholm and the NASA Ames Research Center.

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