PRE–CONFERENCE TUTORIAL

27th Norchip Conference

15 November 2009 at 13.00-17.00, Trondheim, NORWAY

Physical Design and Reliability Issues in Nanoscale Analog CMOS Technologies

Abstract

In nanoscale analog CMOS design there is no good substitute for understanding reliability stress factors or the many effects related to the circuit physical layout which can cause significant design-for-reliability (DFR), performance (DFP), or manufacturability (DFM) yield degradation. Circuit simulation tools presently lack the capability to predict the effect of several stress and reliability effects, including TDDB, HCI, NBTI, etc. Physical design deficiencies found after post-layout-extraction results in re-layout and a waste of the industries most valuable commodity: time to market. This tutorial presents an overview of these effects on nanoscale analog circuit design and also explores how to alter circuit topologies and device geometries to mitigate them. Additionally, methods for extending device terminal voltage limits under certain conditions beyond foundry-specified voltage limits will be explored.

Outline:

13.00 Nanoscale CMOS physical design and device trends
13.30 Device scaling - dimensionless circuit and physical design
14.00 Mitigation of nanoscale device mismatch and C-DAC matching errors
14.40 Nanoscale device reliability issues – digital vs. analog lifetime limits
15.00 Coffee
15.20 Time-dependent dielectric breakdown (TDDB) in startup and standby
15.30 Obtaining additional device voltage headroom in CHE mode
15.50 HCI stress in CHISEL mode – where Vsb>0
16.10 Negative/Positive bias temperature instability (NBTI/PBTI)
16.20 Electromigration (EM) limits on nanoscale CMOS device geometry
16.50 Summary and Conclusions

Sample publications by the Authors:

[1] L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, “Analog Circuit Design in Nanoscale CMOS Technologies,” *Proceedings of the IEEE*, in press.
[2] L. Lewyn, “A Symbolic Method for Scaled CMOS Circuit Design,” *in Proc. IX International Workshop on Symbolic Methods in Analog Circuit Design*, Oct. 2006.
[3] L. Lewyn and J. Meindl, "Physical Limits of VLSI dRAMS," *IEEE J. Solid State Circuits*, Vol. SC-20, pp. 311-321, Feb. 1985.
[4] L. Lewyn and J. Meindl, "An IGFET Inversion Charge Model for VLSI Systems," *IEEE Trans. Electron Devices*, Vol. ED-32, pp. 434-440. Feb. 1985.

Lanny L. Lewyn - B.S. Eng. with honor and M.S.E.E. California Institute of Technology. Ph.D. E.E. Stanford (CIS) 1984. His work at Stanford on physical limits of VLSI circuits resulted in publication of the first closed-form solution for the MOS device surface potential that was continuous from weak to strong inversion.
Past work includes an 18b CMOS DAC design licensed to Toshiba for early 4x OS audio disc players, a 14b CMOS ADC used by DSL industry-pioneers PairGain and Alcatel, and a 1.2 mW, a 16b CMOS ADC x36-array in an image processing ASIC recently installed in the Hubble main survey camera (ACS).
His current work includes overcoming device voltage limitations in nanometer analog CMOS circuits and the design of the next generation >10b 1GSPS 28nm CMOS pipeline ADC IP, including low jitter clock distribution, for the SnowBush IP Division of Gennum, Toronto.
Past positions include Manager, Nuclear Space Instrument Development, NASA-JPL, Director of R&D, Pacemaker Division of American Hospital Supply, Manager, Advanced CMOS Circuit Development, Hughes Solid State Products Division, and Manager, Analog IC Design, PairGain Division of Globespan Inc.
He is currently president of Lewyn Consulting Inc. (LCI) in Laguna Beach, CA, is a course instructor for the Mead Education Group in the subjects of reliability and physical design in nanoscale CMOS technologies, and serves on the technical advisory boards of the Snowbush IP Division of Gennum Physical Design Center, Aguascalientes, Mexico and Tanner EDA, a division of Tanner Research, Monrovia, CA. He is a Life Senior Member of the IEEE and holds 29 U.S. patents in CMOS and bipolar circuits.

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