

INVITED TALKS  
**29th Norchip  
Conference**

14-15 November 2011, Lund, SWEDEN



**Norchip**

### SAW-less Software-Defined Radio Transceivers in 40nm CMOS

The introduction of several new cellular and connectivity radio standards has attracted the wireless industry to the concept of software-defined radio systems, preferably implemented in advanced nanometer CMOS technology. A first generation of transceivers, using several advances in new circuits and architectures, combined with extensive digital compensation techniques, are indeed able to operate over the complete range of both RF frequencies and baseband bandwidths and as such act like an SDR.

However, a real SDR must go further than this. Interoperability and coexistence scenarios, combined with the need to eliminate external fixed-frequency acoustic RF filters, lead to much more stringent requirements on linearity and noise.

Therefore, this paper will also present a novel second generation of 40nm CMOS transceivers that enable this. On the TX side, it is crucial to achieve -160dBc/Hz noise level for all possible combinations of RF frequency, baseband bandwidth, and RX-TX duplex spacing. In the receiver, extremely linear circuits are presented, that are able to handle blockers of around 0dBm input level.

**Jan Craninckx** obtained his Ms. and Ph.D. degree in microelectronics from the Katholieke Universiteit Leuven in 1992 and 1997, respectively. His Ph.D. work was on the design of low-phase noise CMOS integrated VCOs and synthesizers. From 1997 till 2002 he worked with Alcatel Microelectronics as a senior RF engineer on the integration of RF transceivers for GSM, DECT, Bluetooth and WLAN. In 2002 he joined IMEC (Leuven, Belgium), where he currently is the senior principal scientist of the analog wireless research group. His research focuses on the design of RF transceiver front-ends for software defined radio (SDR) systems, covering all aspects of RF, analog and data converter design.

### A new digital signal processing approach

A new digital signal processing approach to shaping inter-symbol-interference (ISI) and static mismatch errors simultaneously in oversampled multi-level digital to analog converters (DAC) has recently been proposed. In this talk, a mathematical framework is established for analyzing ISI errors as well as comparing the ISI sensitivities of different mismatch shaping algorithms. The framework is used to analyze the fundamental problems of popularly used algorithms such as data-weighted-averaging (DWA) in the presence of non-linear ISI: Large-signal even-order distortion and frequency modulated harmonics at low signal levels. The new ISI-shaping algorithm results in significant improvement over previous schemes including the 'modified Mismatch Shaper (MMS)' which also addresses ISI error. The new ISI shaper, while increasing the digital complexity, practically eliminates the need for conventional ISI mitigation techniques such as time consuming, layout-critical, non-automated and process specific analog design methods. The advantages of ISI shaping is further verified on an experimental audio DAC with simple Non-Return-to-Zero (NRZ) current steering segments implemented in a 45nm CMOS process and running off a single-phase clock of only 3.072MHz.

**Lars Risbo** received both his M.Sc.EE (1991) and Ph.D (1994) degrees from the Technical University of Denmark. Both Thesis works were on stability analysis and loop synthesis of high-order Sigma-Delta Modulators. He founded Toccata Technology in 1996 where he developed the world's first true digital power amplifier (1998) based on digital PCM to PWM conversion and a switching power stage (recognized in the Guinness book of records 1999). After Texas instruments acquired Toccata, he drove the development of the successful and market leading TI PurePath digital audio amplifier devices (TASXXXX family). He is currently serving as Distinguished Member of the Technical Staff in the Audio and Imaging Products group at TI in Lyngby, Denmark.

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### Efficiency and flexibility

Scaling of CMOS technology is no longer beneficial for energy reduction as it was in the past. To mitigate process variations and leakage, voltage scaling has slowed down. At the same time, increasing application diversity and increasing complexity require great amounts of flexibility in digital hardware within constrained energy. These changes in process technology and applications are now placing new emphasis on design. Custom chips are becoming too costly, programmable chips overrun energy budget. This talk will therefore present a solution to this problem. Radix factorization algorithms will be applied at varying levels of complexity. To gain insight into chip-level ideas, FFT factorization will be shown to achieve record energy and area efficiency. These insights will carry over to chip-level interconnect architecture and show that flexibility and efficiency can exist in the same chip. New technologies that scale better than CMOS in supporting architectural features will be explored.

**Dejan Marković** is an Assistant Professor of Electrical Engineering at the University of California, Los Angeles. He completed the Ph.D. degree in 2006 at the University of California, Berkeley. In recognition of the impact of his Ph.D. work, he was awarded 2007 David J. Sakrison Memorial Prize at UC Berkeley. His current research is focused on integrated circuits for emerging radio and healthcare systems, programmable ICs, design with post-CMOS devices, optimization methods and CAD flows. He received an NSF CAREER Award in 2009. In 2010, he was a co-recipient of ISSCC Jack Raper Award for Outstanding Technology Directions and a winner of the DAC/ISSCC Student Design Contest.

### A 90nm RFCMOS radio supports 9 WCDMA/EDGE bands with full RX diversity

The 2G RX/TX + LO consumes 129mW/126mW, while the 3G TX+RX+LO consumes 269mW. The SAW-less 2G/3G RX has an NF of 2.3-2.5dB, with IIP2 > +58dBm and IIP3 > -6dBm. The 2G TX EVM is below 1.5% thanks to the use of a polar TX architecture with a two-point PLL, while the 3G TX EVM is below 4%. The RX EVM is below 3%. The transceiver occupies a die area of  $3.78 \times 3.78\text{mm}^2$ .

**Magnus Nilsson** received his MS degree in electrical engineering from Lund University in 1994. In 1995 he started at Ericsson, then continued at Ericsson Mobile Platforms in 2002 and is since 2009 working at ST-Ericsson. He is currently working as RFIC technical lead and holds more than 10 patents in the RFIC area.

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