## MONDAY 12 NOVEMBER 2012

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<tr>
<th>Time</th>
<th>Session</th>
<th>Speaker(s)/Institution</th>
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<td>09:00</td>
<td>Opening and welcome</td>
<td>Erik Bruun, Technical University of Denmark (DK)</td>
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<tr>
<td>09:15</td>
<td>Invited talk: Nanoscale CMOS Impulse Radar - From Research to Product</td>
<td>Dag Wisland, Novelda (NO)</td>
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<td>10:00</td>
<td>Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications</td>
<td>Jonas Stenbæk Hegner, Joakim Sindholt and Alberto Nannarelli, Technical University of Denmark (DK)</td>
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<tr>
<td>10:20</td>
<td>Architectural Trends in GHz Speed DACs</td>
<td>Sidharth Balasubramanian and Waleed Khalil, Ohio State University (US)</td>
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<td>11:10</td>
<td>A Continuous-Time IR-UWB RAKE Receiver for Coherent Symbol Detection</td>
<td>Shanthi Sudalaiyandi and Tor Sverre Lande, University of Oslo (NO)</td>
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<td>11:30</td>
<td>A Power Scalable and High Pulse Swing UWB Transmitter for Wireless-Powered RFID Applications</td>
<td>Jia Mao, Zhuo Zou, David Sarmiento Mendoza, Fredrik Jonsson and Li-Rong Zheng, Royal Institute of Technology (SE)</td>
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<td>11:50</td>
<td>A 26 GHz UWB CMOS IR-UWB Transmitter with On-chip Balun</td>
<td>Kristian Gjertsen Kjelgård and Tor Sverre Lande, University of Oslo (NO)</td>
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<td>12:10</td>
<td>Lunch</td>
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<td>13:30</td>
<td>Invited talk: Challenges in IC Design for Hearing Aids</td>
<td>Ivan Jørgensen, Technical University of Denmark (DK)</td>
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<td>Modeling and Design of a Dual-Residue Pipelined ADC in 130nm CMOS</td>
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### 1.1 Ultra Wide Band Systems

**CHAIR:** Dag T. Wisland, University of Oslo (NO)

**11:10** A Continuous-Time IR-UWB RAKE Receiver for Coherent Symbol Detection
Shanthi Sudalaiyandi and Tor Sverre Lande, University of Oslo (NO)

**11:30** A Power Scalable and High Pulse Swing UWB Transmitter for Wireless-Powered RFID Applications
Jia Mao, Zhuo Zou, David Sarmiento Mendoza, Fredrik Jonsson and Li-Rong Zheng, Royal Institute of Technology (SE)

**11:50** A 26 GHz UWB CMOS IR-UWB Transmitter with On-chip Balun
Kristian Gjertsen Kjelgård and Tor Sverre Lande, University of Oslo (NO)

### 1.2 FPGA Based Accelerators

**CHAIR:** Alberto Nannarelli, Technical University of Denmark (DK)

**11:10** H.264/AVC Motion Estimation on FPGAs and GPUs: A Comparative Study
Iraçu O. Santos1,3, Alba S. B. Lopes2, Bruno M. Carvalho3, Edgard Correia and Marcio Kreutz1,1UFPA (BR), 2IFRN (BR), 3DIMAp-UFRN (BR)

**11:30** FPGA Implementation of Elementary Generalized Unitary Rotation with CORDIC Based Architecture
Peteris Misans, Uldis Derums and Vents Kanders, Riga Technical University (LV)

**11:50** Energy Efficient MIMO Channel Pre-processor Using a Low Complexity On-Line Update Scheme
Chenxin Zhang, Hemanth Prabhu, Liang Liu, Ove Edfors and Viktor Öwall, Lund University (SE)

**12:10** Lunch

**13:30** Invited talk: Challenges in IC Design for Hearing Aids
Ivan Jørgensen, Technical University of Denmark (DK)

**14:15** Modeling and Design of a Dual-Residue Pipelined ADC in 130nm CMOS
A 9-bit 50MS/s Asynchronous SAR ADC in 28nm CMOS
Tuan-Vu Cao, Snorre Aunet, Trond Ytterdal, Norwegian University of Science and Technology (NO)

2.2 Circuit and Architecture Synthesis
CHAIR: Viktor Öwall, Lund University (SE)

Optimal Register Allocation by Augmented Left-Edge Algorithm on Arbitrary Control-Flow Structures
Mark Ruvald Pedersen and Jan Madsen, Technical University of Denmark (DK)

4.1 Low Power Circuits
CHAIR: Alberto Nannarelli, Technical University of Denmark (DK)

Behavioral Modeling of Nonlinear Settling for Multiple Cascaded SC Stages
Jia Sun, Timo Rahkonen and Marko Neitola, University of Oulu (FI)

A Readout Circuit for an Uncooled IR Camera With Mismatch and Self-Heating Compensation
Daniel Svärd, Christer Jansson and Attila Alvandpour, Linköping University (SE)

Embedded Low Power Clock Generator for Sensor Nodes
Oliver Schrape and Frank Vater, IHP (DE)

Wideband RF Detector Design for High Performance On-Chip Test
Quoc-Tai Duong and Jerzy J. Dąbrowski, Linköping University (SE)

Effect of process variations in CMOS chips for radar beamforming
Elias Bakken, Tor Sverre Lande and Sverre Holm, University of Oslo (NO)

SynZEN: A Hybrid TTA/VLIW Architecture with a Distributed Register File
Stefan Hauser, Nico Moser and Ben Juurlink, Technische Universität Berlin (DE)

A Fault-Aware Low-Energy Core Allocation in Networks-on-Chip
Fatemeh Khalili, Hamid R. Zarrandi, Amirkabir University of Technology (Tehran Polytechnic) (IR)

An Accurate Fault Location Method Based on Configuration Bitstream Analysis
Zhou Jing, Liu Zengrong, Chen Lei, Wang Shuo, Wen Zhiping, Chen Xun and Qi Chang, Beijing Microelectronics Technology Institution (CN)

16:20 Variability-aware design of 55 nA current reference with 1.37% standard deviation and 290 nW power consumption
Francesca Cucchi, Stefano Di Pascoli and Giuseppe Iannaccone Università di Pisa (IT)

16:00 Memory-Aware System Scenario Approach Energy Impact
Iason Filippopoulos1, Francky Cathoor2, Per Gunnar Kjeldsberg1, Elena Humari1 and Jos Huisken2, 1Norwegian University of Science and Technology (NO), 2IMEC (BE)

16:20 Configurable RTL Model for Level-1 Caches
Vahid Saljooghi, Alen Bardizbanyan, Magnus Själander and Per Larsson-Edefors, Chalmers University of Technology (SE)

16:40 Novel SRAM Bias Control Circuits for a Low Power L1 Data Cache
Azam Seyedi1,2, Adrià Armejach1,2, Adrián Cristal1,3, Osman S. Unsal1 and Mateo Valerol1, IBSC Microsoft Research Centre
**Tuesday 13 November 2012**

09:00 Invited talk: Electrical and Human Feedback  
**Hanspeter Schmid, University of Applied Sciences Northwestern Switzerland**

5.1 **Amplifiers**  
**CHAIR:** Kari Halonen, Aalto University (FI)

09:45 An Operational Amplifier for High Performance Pipelined ADCs in 65nm CMOS  
**Sima Payami and Amin Ojani, Linköping University (SE)**

10:05 Analyses of Single-Stage Complementary Self-Biased CMOS Differential Amplifiers  
**Vladimir Milovanović and Horst Zimmermann, Vienna University of Technology (AT)**

6. **Poster Session II**

10:25 Coffee / Poster Session

Lithography analysis of via-configurable transistor-array fabrics  
**Vinicius Dal Bem, André I. Reis, Renato P. Ribas, Institute of Informatics, UFRGS (BR)**

Evaluation of SU8 Photo Polymer for Microwave Packaging Applications  
**Srinivasa Reddy Kuppreddi1, Sayanu Pamidighantam2, V. Janardhana3, Oddvar Sorasen1, J. S. Roy3 and R. G. Kulkarn4, 1University Of Oslo (NO), 2P. E. S Institute of Technology (IN), 3Birla Institute of Technology (IN), 4Bharat Electronics Limited (IN)**

5.2 **Radar Systems**  
**CHAIR:** Johnny Öberg, Royal Institute of Technology (SE)

09:45 Heart and Respiratory Detection and Simulations for Tracking Humans based on Respiration by using Pulse-Based Radar  
**Mehran Baboli, Olga Boric-Lubecke and Victor Lubeckel, University of Hawaii (US)**

10:05 Implementation of FPGA Based DSP Module for CW Doppler radar: Preliminary results  
**Maris Terauds, Riga Technical University (LV)**

A Survey on Mixed Operating Mode/Self Synchronization  
**Dipak S. Marathe, A. C. Patil College of Engineering (IN)**

Integration of TTA processor tools to Kactus2 IP-XACT design flow  
**Lauri Mattilainen, Sakari Lahti, Otto Esko, Erno Salminen and Timo D. Hämmäläinen, Tampere University of Technology (FI)**

7.1 **Data Converters and Time-to-Digital Converters**  
**CHAIR:** Dag T. Wisland, University of Oslo (NO)

11:10 A 2.1μW 76 dB SNDR DT-ΔΣ Modulator for Medical Implant Devices  
**Ali Fazli Yeknami and Atila Alvandpour, Linköping University (SE)**

11:30 Power efficient arrangement of Oversampling Sigma Delta DAC  
**Nadeem Afzal and J. Jacob Wikner, Linköping University (SE)**

11:50 A 90nm CMOS Gated-Ring-Oscillator-Based 2-Dimension Vernier Time-to-Digital Converter  
**Ping Lu1, Pietro Andreani1, Antonio Liscidini2, 1 Lund University (SE), 2Pavia University (IT)**

7.2 **Bio-Inspired and Reliable Systems**  
**CHAIR:** Jan Madsen, Technical University of Denmark (DK)

11:10 Study and Simulation of an Example Redundant FIR Filter  
**PathAware: A Contention-aware Selection Function for Application-specific Network-on-Chips**  
**Behrad Niazmand, Midia Reshadi and Akram Reza, Islamic Azad University (IR)**
8.1 RF Circuits
CHAIR: Tor S. Lande, University of Oslo (NO)

13:55 Linearization of RF Power Amplifiers Using an Enhanced Memory Polynomial Predistorter
Felice Francesco Tafuri1, Cataldo Guaragnella2, Marco Fiore3 and Torben Larsen1, 1Aalborg University (DK), 2Politecnico di Bari (IT), 3Elettronika s.r.l. (IT)

14:15 Deembedding Static Nonlinearities of Power Amplifiers Using Least Square Error Algorithm
Wei Wei, Jan H. Mikkelsen and Ole Kiel Jensen, Aalborg University (DK)

8.2 NoC Design and Optimization
CHAIR: Peeter Ellervee, Tallinn University of Technology (EE)

13:55 Testing of an off-chip NoC protocol using a BIST/Synthesizable Testbench approach
Saif Uddin and Johnny Öberg, Royal Institute of Technology (SE)

14:15 A Light-Weight Statically Scheduled Network-on-Chip
Rasmus Bo Sorensen, Martin Schoebert, Jens Sparso, Technical University of Denmark (DK)

14:35 Intermediate Nodes Selection Schemes for Network Coding in Network-on-Chips
Ahmed Mohamed Shalaby, Mohamed El-Sayed Ragab and Victor Mauro Goulart, Egypt-Japan University of Science and Technology (EG)

14:55 A Genetic Algorithm based Optimization Method for Low Vertical Link Density 3-Dimensional Networks-on-Chip Many Core Systems
Haoyuan Ying, Kris Heid, Thomas Hollstein and Klaus Hofmann, Darmstadt University of Technology (DE)

15:15 Closing remarks and NORCHIP 2013

SESSION ORGANISATION
Both oral and poster presentations have been carefully selected through a regular review process and they will all appear in the proceedings. Equal quality measures have been applied to posters and lectures. Papers for oral presentation are selected based on thematic composition of sessions.

PROCEEDINGS
USB stick proceedings of the conference contributions will be distributed upon registration. Each participant will receive a copy of the proceedings. Proceedings and all presentations will be in English.

BEST ANALOG PAPERS
The Management Committee has since 1992 made special issues of the Springer International Journal on Analog Integrated Circuits and Signal Processing. Also this year we will publish a number of the best analog papers in the journal.
http://www.springer.com/engineering/circuits+%26+systems/journal/10470

BEST DIGITAL PAPERS
The best digital papers will be invited to publish in the international Elsevier journal Embedded Hardware Design (MICPRO).
http://www.elsevier.com/wps/find/journaldescription.cws_home/525449/description#description
General Scope of the Conference
The NORCHIP conference is the main microelectronics event of the Nordic countries. The annual IEEE CAS sponsored conference covers all areas of microelectronics, spanning from large digital systems to simple analog circuits. The wide scope of NORCHIP is intentional promoting cross-field collaboration. NORCHIP is a well established conference with representation from both academia and industry. Papers of the highest scientific and technical quality are presented together with selected invited speakers and pre-conference tutorial sessions.

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- Jan Madsen, Technical University of Denmark (DK)
- Viktor Öwall, Lund University (SE)
- Attila Alvandpour, Linköping University (SE)
- Jari Nurmi, Tampere University of Technology (FI)
- Peeter Ellerbee, Tallinn Univ. of Technology (EE)

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- Erik Bruun, Technical University of Denmark (DK)
- Jan Madsen, Technical University of Denmark (DK)

Conference Venue / Accommodation
The conference location is in the heart of Copenhagen at:
Hotel Richmond
Vester Farimagsgade 33
DK-1606 Copenhagen V

www.profilhotels.dk/richmondhotel/

Registration
The registration form on www.norchip.org must be completed and returned to the Conference Secretariat, together with full payment. The registration fee of EUR 480 includes proceedings, banquet dinner, lunches and coffee breaks. Registration deadline is 26 October. Registrations are acknowledged upon reception.