<table>
<thead>
<tr>
<th>Time</th>
<th>Session/Workshop</th>
<th>Chair</th>
</tr>
</thead>
<tbody>
<tr>
<td>09:00</td>
<td>Opening and welcome</td>
<td>Erik Bruun, Technical University of Denmark (DK)</td>
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<tr>
<td>09:15</td>
<td>Invited talk: Nanoscale CMOS Impulse Radar - From Research to Product</td>
<td>Dag Wisland, Novelda (NO)</td>
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<tr>
<td>10:00</td>
<td>Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications</td>
<td>Jonas Stenbæk Hegner, Joakim Sindholt and Alberto Nannarelli, Technical University of Denmark (DK)</td>
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<tr>
<td>10:20</td>
<td>Architectural Trends in GHz Speed DACs</td>
<td>Sidharth Balasubramanian and Waleed Khalil, Ohio State University (US)</td>
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<tr>
<td>11:10</td>
<td>A Continuous-Time IR-UWB RAKE Receiver for Coherent Symbol Detection</td>
<td>Shanthi Sudalaiyandi and Tor Sverre Lande, University of Oslo (NO)</td>
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<td>11:30</td>
<td>A Power Scalable and High Pulse Swing UWB Transmitter for Wirelessly-Powered RFID Applications</td>
<td>Jia Mao, Zhuo Zou, David Sarmiento Mendoza, Fredrik Jonsson and Li-Rong Zheng, Royal Institute of Technology (SE)</td>
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<td>11:50</td>
<td>A 26 GHz UWB CMOS IR-UWB Transmitter with On-chip Balun</td>
<td>Kristian Gjertsen Kjelgård and Tor Sverre Lande, University of Oslo (NO)</td>
</tr>
<tr>
<td>11:10</td>
<td>H.264/AVC Motion Estimation on FPGAs and GPUs: A Comparative Study</td>
<td>Iraçu O. Santos1,3, Alba S. B. Lopes2, Bruno M. Carvalho3, Edgard Correa3 and Marcio Kreutz1, 1UFPA (BR), 2IFRN (BR), 3DIMAp-UFRN (BR)</td>
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<td>11:30</td>
<td>FPGA Implementation of Elementary Generalized Unitary Rotation with CORDIC Based Architecture</td>
<td>Peteris Misans, Uldis Derums and Vents Kanders, Riga Technical University (LV)</td>
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<td>11:50</td>
<td>Energy Efficient MIMO Channel Pre-processor Using a Low Complexity On-Line Update Scheme</td>
<td>Chenxin Zhang, Hemanth Prabhu, Liang Liu, Ove Edfors and Viktor Öwall, Lund University (SE)</td>
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<td>12:10</td>
<td>Lunch</td>
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<tr>
<td>13:30</td>
<td>Invited talk: Challenges in IC Design for Hearing Aids</td>
<td>Ivan Jørgensen, Technical University of Denmark (DK)</td>
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<tr>
<td>14:15</td>
<td>Modeling and Design of a Dual-Residue Pipelined ADC in 130nm CMOS</td>
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</table>

**1.1 Ultra Wide Band Systems**

**1.2 FPGA Based Accelerators**

**2.1 Nyquist-Rate A/D Converters**
2. Circuit and Architecture Synthesis

CHAIR: ?

14:15  KL-Cut Based Mapped Circuits Remapping
Lucas Machado, Mayler Martins, inicius Callegaro, Renato P. Ribas and André I. Reis, Institute of Informatics, UFRGS (BR)

14:35  Optimal Register Allocation by Augmented Left-Edge Algorithm on Arbitrary Control-Flow Structures
Mark Ruvald Pedersen and Jan Madsen, Technical University of Denmark (DK)

3. Poster Session I

14:55  Coffee / Poster Session

Behavioral Modeling of Nonlinear Settling for Multiple Cascaded SC Stages
Jia Sun, Timo Rahkonen and Marko Neitola, University of Oulu (FI)

An Analog Receiver Front-End for Capacitive Body-Coupled Communication
Prakash Harikumar, Muhammad Irfan Kazim and Jacob Wikner, Linköping University (SE)

A Readout Circuit for an Uncooled IR Camera With Mismatch and Self-Heating Compensation
Daniel Svärd, Christer Jansson and Atila Alvandpour, Linköping University (SE)

15:00  Embedded Low Power Clock Generator for Sensor Nodes
Oliver Schrape and Frank Vater, IHP (DE)

15:15  Wideband RF Detector Design for High Performance On-Chip Test
Quoc-Tai Duong and Jerzy J. Dąbrowski, Linköping University (SE)

Effect of process variations in CMOS chips for radar beamforming
Elias Bakken, Tor Sverre Lande and Sverre Holm, University of Oslo (NO)

SynZEN: A Hybrid TTA/VLIW Architecture with a Distributed Register File
Stefan Hauser, Nico Moser and Ben Juurlink, Technische Universität Berlin (DE)

A Fault-Aware Low-Energy Spare Core Allocation in Networks-on-Chip
Fatemeh Khalili, Hamid R. Zariandi, Amirkabir University of Technology (Tehran Polytechnic) (IR)

An Accurate Fault Location Method Based on Configuration Bitstream Analysis
Zhou Jing, Liu Zengrong, Chen Lei, Wang Shuo, Wen Zhiping, Chen Xin and Qi Chang, Beijing Microelectronics Technology Institution (CN)

4.1 Low Power Circuits

CHAIR: ?

16:00  A Novel On-Chip Ultra-low Power Temperature Sensing Scheme
Shailesh Singh Chouhan and Kari Halonen, Aalto University (FI)

16:20  Variability-aware design of 55 nA current reference with 1.37% standard deviation and 290 nW power consumption
Francesca Cucchi, Stefano Di Pascoli and Giuseppe Iannaccone Università di Pisa (IT)

16:40  Low Power Real Time Clock With High Accuracy Over Large Supply Voltage Range
Wolfgang Gut, Gerald Hilber, Dominik Gruber, Manuel Kaufmann, Andreas Rauchenecker and Timm Ostermann, Johannes Kepler University of Linz (AT)

4.2 Memory Design and Optimization

CHAIR: ?

16:00  Memory-Aware System Scenario Approach Energy Impact
Iason Filippopoulos1, Francy Catthoor2, Per Gunnar Kjeldsberg1, Elena Hammari1 and Jos Huisken2, Norwegian University of Science and Technology (NO), 2IMEC (BE)

16:20  Configurable RTL Model for Level-1 Caches
Vahid Saljooghi, Alen Bardizbanyan, Magnus Sjölander and Per Larsson-Edefors, Chalmers University of Technology (SE)

16:40  Novel SRAM Bias Control Circuits for a Low Power L1 Data Cache
Azam Seyedi1,2, Adria Armejach1,2, Adrián Cristal1,3, Osman S. Unsal1 and Mateo Valero1, 1BSC Microsoft Research Centre (ES), 2Universitat Politècnica de Catalunya (ES), 3Spanish National Research Council (ES)

19.00  Dinner
09:00 Invited talk: Electrical and Human Feedback
Hanspeter Schmid, University of Applied Sciences Northwestern Switzerland

5.1 Amplifiers
CHAIR: ?
09:45 An Operational Amplifier for High Performance Pipelined ADCs in 65nm CMOS
Sima Payami and Amin Ojani, Linköping University (SE)

10:05 Analyses of Single-Stage Complementary Self-Biased CMOS Differential Amplifiers
Vladimir Milovanović and Horst Zimmermann, Vienna University of Technology (AT)

5.2 Radar Systems
CHAIR: ?
09:45 Heart and Respiratory Detection and Simulations for Tracking Humans based on Respiration by using Pulse-Based Radar
Mehran Baboli, Olga Boric-Lubecke and Victor Lubeckel, University of Hawaii (US)

10:05 Implementation of FPGA Based DSP Module for CW Doppler radar: Preliminary results
Maris Terauds, Riga Technical University (LV)

6. Poster Session II
10:25 Coffee / Poster Session

Lithography analysis of via-configurable transistor-array fabrics
Vinicius Dal Bem, André I. Reis, Renato P. Ribas, Institute of Informatics, UFRGS (BR)

Evaluation of SU8 Photo Polymer for Microwawe Packaging Applications
Srinivasa Reddy Kuppireddi1, Sayanu Pami, Gighamant, V. Janardhana3, Odvar Sorasen1, J.S. Roy3 and R.G. Kulkarn4, 1University Of Oslo (NO), 2P.E.S Institute of Technology (IN), 3Birla Institute of Technology (IN), 4Bharat Electronics Limited (IN)

A Measurement Technique for the Vibrating Wire Sensors
Andrea Simonetti and Alessandro Trifiletti, University of Rome “La Sapienza” (IT)

Functional Built-In Self-Test for Processor Cores in SoC
Raimund Ubar, Viljar Indus, Oliver Kalmend and Teet Evarton, Tallinn University of Technology (EE)

PathAware: A Contention-aware Selection Function for Application-specific Network-on-Chips
Behrad Niazmand, Midia Reshadi and Akram Reza, Islamic Azad University (IR)

A Survey on Mixed Operating Mode/Self Synchronization
Dipak S. Marathe, A.C. Patil College of Engineering (IN)

Integration of TTA processor tools to Kactus2 IP-XACT design flow

7. Data Converters and Time-to-Digital Converters
CHAIR: ?
11:10 A 2.1μW 76 dB SNDR DT-ΔΣ Modulator for Medical Implant Devices
Ali Fazli Yeknami and Atila Alvandpour, Linköping University (SE)

11:30 Power efficient arrangement of Oversampling Sigma Delta DAC
Nadeem Afzal and J. Jacob Wikner, Linköping University (SE)

11:50 A 90nm CMOS Gated-Ring-Oscillator-Based 2-Dimension Vernier Time-to-Digital Converter
Ping Lai1, Pietro Andreani1, Antonio Liscidin12, 1 Lund University (SE), 2Pavia University (IT)

7.2 Bio-Inspired and Reliable Systems
CHAIR: ?
11:10 Study and Simulation of an Example Redundant FIR Filter
Joakim Alvbrant and J. Jacob Wikner, Linköping University (SE)

11:30 Artificial Neural Network Emulation on NOC based Multi-Core FPGA Platform
Nowshad Painda Mand, Francesco Robino and Johnny Öberg, Royal Institute of Technology (SE)
11:50 Performance of Error Control Schemes for NOC Interconnects
Deena M. Zamzam1, Mohamed A. Abd El Ghany1,2, Klaus Hofmann2, 1German University in Cairo (EG), 2Darmstadt University of Technology (DE)

12:10 Lunch

13:10 Invited talk: Biochips: The Integrated Circuit of Biology
Jan Madsen, Technical University of Denmark (DK)

8.1 RF Circuits
CHAIR: ?

13:55 Linearization of RF Power Amplifiers Using an Enhanced Memory Polynomial Predistorter
Felice Francesco Tafuri1, Cataldo Guaragnella2, Marco Fiore3 and Torben Larsen1, 1Aalborg University (DK), 2Politecnico di Bari (IT), 3Elettronica s.r.l. (IT)

14:15 Deembedding Static Nonlinearities of Power Amplifiers Using Least Square Error Algorithm
Wei Wei, Jan H. Mikkelsen and Ole Kiel Jensen, Aalborg University (DK)

14:35 Wideband Reconfigurable Capacitive Shunt-Feedback LNA in 65nm CMOS
Imad ud Din, Johan Wernehag, Stefan Andersson and Sven Mattisson, Ericsson Research (SE)

14:55 A 2.5 GHz Self-Compensated, Bandwidth Tracking PLL with 0.8 ps Jitter

Mitesh Yogesh1, Puneet Sareen2, Markus Dietl2 and Ketan Dewan2, 1Linköping University (SE), 2Texas Instruments (DE)

8.2 NoC Design and Optimization
CHAIR: ?

13:55 Testing of an off-chip NoC protocol using a BIST/Synthesizable Testbench approach
Saif Uddin and Johnny Öberg, Royal Institute of Technology (SE)

14:15 A Light-Weight Statically Scheduled Network-on-Chip
Rasmus Bo Sørensen, Martin Schoeberl, Jens Sparso, Technical University of Denmark (DK)

14:35 Intermediate Nodes Selection Schemes for Network Coding in Network-on-Chips
Ahmed Mohamed Shalaby, Mohamed El-Sayed Ragab and Victor Mauro Goulart, Egypt-Japan University of Science and Technology (EG)

14:55 A Genetic Algorithm based Optimization Method for Low Vertical Link Density 3-Dimensional Networks-on-Chip Many Core Systems
Haoyuan Ying, Kris Heid, Thomas Hollstein and Klaus Hofmann, Darmstadt University of Technology (DE)

15:15 Closing remarks and NORCHIP 2013

SESSION ORGANISATION
Both oral and poster presentations have been carefully selected through a regular review process and they will all appear in the proceedings. Equal quality measures have been applied to posters and lectures. Papers for oral presentation are selected based on thematic composition of sessions.

PROCEEDINGS
USB stick proceedings of the conference contributions will be distributed upon registration. Each participant will receive a copy of the proceedings. Proceedings and all presentations will be in English.

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The Management Committee has since 1992 made special issues of the Springer International Journal on Analog Integrated Circuits and Signal Processing. Also this year we will publish a number of the best analog papers in the journal.
http://www.springer.com/engineering/circuits+%26+systems/journal/10470

BEST DIGITAL PAPERS
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http://www.elsevier.com/wps/find/journaldescription.cws_home/525449/description#description

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The NORCHIP conference is the main microelectronics event of the Nordic countries. The annual IEEE CAS sponsored conference covers all areas of microelectronics, spanning from large digital systems to simple analog circuits. The wide scope of NORCHIP is intentional promoting cross-field collaboration. NORCHIP is a well established conference with representation from both academia and industry. Papers of the highest scientific and technical quality are presented together with selected invited speakers and pre-conference tutorial sessions.
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Vester Farimagsgade 33  
DK-1606 Copenhagen V  
www.profilhotels.dk/richmondhotel/

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