Tampere, Finland
15-16 November 2010

Norchip
THE NORDIC MICROELECTRONICS EVENT

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IEEE CAS

CONFERENCE SECRETARIAT

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MONDAY 15 NOVEMBER 2010

09.00 Opening and welcome
Jari Nurmi, Tampere Univ. of Technology (FI)

09.15 Invited talk: Testing and Design-for-Testability Techniques for 3D Integrated Circuits
Krishnendu Chakrabarty, Duke University (US)

10.00 Ultra Low Energy vs Throughput Design Exploration of 65 nm Sub-VT CMOS Digital Filters
Syed Muhammad Yasser Sherazi et al, Lund University (SE)

10.20 Research and Practices on 3D Networks-on-Chip Architectures
Amir-Mohammad Rahmani et al, University of Turku (FI)

10.40 Coffee

1.1 ANALOG CIRCUITS
CHAIR: MARKKU ÅBERG, VTT (FI)

11.10 A Low Power Analog Channel Decoder for Ultra Portable Devices in 65 nm Technology
Reza Meraji et al, Lund University (SE)

11.30 Analog Baseband Chain of Synthetic Array Radar (SAR) Receiver
Faizah Abu Bakar et al, Aalto University (FI)

11.50 A 900 MHz 10 mW Monolithically Integrated Inverse Class E Power Amplifier
Jukka Typpö, NTNU (NO)

1.2 MEMORY ARCHITECTURE
CHAIR: VIKTOR ÖWALL, LUND UNIVERSITY (SE)

11.10 An Analysis of Designing 2D/3D Chip Multiprocessor with Different Cache Architecture
Thomas Canhao Xu et al, University of Turku (FI)

11.30 A NoC Based Distributed Memory Architecture with Programmable and Partitionable Capabilities
Muhammad Adeel Tajammul et al, Royal Institute of Technology (SE)

11.50 On Power and Performance Tradeoff of L2 Cache Compression
Tom Chen et al, Colorado State University (US)

12.10 Lunch

13.30 Invited talk: Towards self-powered biomedical devices
Yong Lian, National University of Singapore

2.1 D/A CONVERTERS
CHAIR: ERIK BRUUN, TECHNICAL UNIV. OF DENMARK

14.15 Effects of Filtering on the Linearity of Current-steering IF DAC
Timo Rahkonen et al, Oulu University (FI)

14.35 A Higher Nyquist-Range DAC Employing Sinusoidal Interpolation
Reza Sadeghifar et al, Linköping University (SE)

2.2 HIGH-LEVEL MODELING
CHAIR: GERT JERVAN, TALLINN UNIV. OF TECHN. (EE)

14.15 Execution Models for Processors and Instructions
Florian Brandner et al, ENS de Lyon (FR)

14.35 Analysis of Modeling Styles on Network-on-Chip Simulation
Lasse Lehtonen et al, Tampere Univ. of Technology (FI)

3. POSTER SESSION I
14.55 Coffee / Poster session:

High Level Synthesis Framework For a Coarse Grain Reconfigurable Architecture
Omer Malik et al, Royal Institute of Technology (SE)

Designing a dataflow processor using ClaSH
Anja Niedermeier et al, University of Twente (NL)

An Improved Hardware Acceleration Scheme for Java Method Calls
Tero Säntti et al, University of Turku (FI)

Exploration of Target Architecture for a Wireless Camera Based Sensor Node
Muhammad Imran et al, Mid Sweden University (SE)

FPGA-based Real-Time Disparity Computation and Object Location
Pedro Miguel Santos et al, Universidade do Porto (PT)

Application Of Medium-Grain Multiprocessor Mapping Methodology To Epileptic Seizure Predictor
Elena HAMMARI et al, NTNU (NO)

DLL based temperature compensated MEMS clock
Arto Rantala et al, VTT Finland (FI)

Modeling of Peak-to-peak Switching Noise along a Vertical Chain of Power Distribution TSV pairs in a 3D Stack of ICs interconnected through TSVs
Waqar Ahmad et al, Royal Institute of Technology (SE)

A Fast and Accurate Phase Noise Measurement of Free Running Oscillators Using a Single Spectrum Analyzer
JIan Chen et al, Royal Institute of Technology (SE)

A Novel Simple and High Performance Structure for Improving CMRR: Application to Current Buffers and Folded Cascode Amplifier
Amir Hossein Miremadi et al, Islamic Azad Univ. (IR)

A Low-Power, Medium-Resolution, High-Speed CMOS Pipelined ADC
Deivasigamani Meganathan,

Dimensioning Space of a Parallel Tuned Amplifier
Simo Hietakangas, University of Oulu (FI)

A Self-Oscillating LNA-Mixer
Tero Koivisto et al, University of Turku (FI)

A New DFT based Approach for Gain Mismatch Detection and Correction in Time-Interleaved ADCs
Yashar Hesamiafshar et al, Urmia University (IR)

Developments of the SoC for High-Multi-Level QAM 1 Gbps Class Wireless System and its Evaluation with RF Hardware of 38 GHz Band FWA
Toru Taniguchi et al, Japan Radio Co (JP)

Study of Modified Noise-Shaper Architectures for Oversampled Sigma-Delta DACs
Nadeem Afzal et al, Linköping University (SE)

Hierarchical Power Monitoring on NoC - A Case Study for Hierarchical Agent Monitoring Design Approach
Liang Guang et al, University of Turku (FI)

4.1 RF: LOW-NOISE AMPLIFIERS

CHAIR: HENRIK SJÖLAND, LUND UNIVERSITY (SE)

16.00 A DC-Invariant Gain Control Technique for CMOS Differential Variable-Gain Low-Noise Amplifiers
Muh-Dey Wei et al, Aachen University (DE)

16.20 A Small-Area Self-Biased Wideband CMOS Balun LNA with Noise Cancelling and Gain Enhancement
J. R. Custódio et al, Univ. Nova de Lisboa (PT)

16.40 Wideband Inductorless LNA Employing Simultaneous 2nd and 3rd Order Distortion Cancellation
Omid E Najari et al, Linköping University (SE)

4.2 MANYCORE SYSTEMS

CHAIR: JARI NURMI, TAMPERE UNIV. OF TECHN. (FI)

16.00 Multi-Application Multi-Step Mapping Method for Many-Core Network-on-Chips
Bo Yang et al, University of Turku (FI)

16.20 Multi-FPGA Implementation of a Network-on-Chip Based Many-core Architecture with Fast Barrier Synchronization Mechanism
Xiaowen Chen et al, Royal Inst. of Techn. (SE)

16.40 Latency Reduction of Selected Data Streams in Network-on-Chips for Adaptive Manycore Systems
Thilo Pionteck et al, Universität zu Lübeck (DE)

19.00 Dinner

TUESDAY 16 NOVEMBER 2010

09.00 Invited talk: Sensor Processing And Power Management in Smartphone Platforms
Lasse Harju, ST-Ericsson (FI)

5.1 TIME-TO-DIGITAL CONVERTERS

CHAIR: KARI HALONEN, AALTO UNIVERSITY (FI)

09.45 A High-resolution Vernier Gated-Ring-Oscillator TDC in 90-nm CMOS
Ping Lu et al, Lund University (SE)

10.05 A 12-Bit Digital-to-Time Converter (DTC) for Time-to-Digital Converter (TDC) and other Time Domain Signal Processing Applications
Salim Alahdab et al, University of Oulu (FI)

5.2 FPGA APPLICATIONS

CHAIR: VIKTOR ÖWALL, LUND UNIVERSITY (SE)

09.45 Exploring FPGAs Capability to Host a HPC Design
Clement Foucher et al, Université de Nice-Sophia Antipolis (FR)

10.05 Flexible Hardware Implementation of Collaborative GNSS Tracking Channel

Heikki Hurskainen et al, Tampere Univ. of Technology (FI)

6. POSTER SESSION II

10.25 **Coffee / Poster session:**

Simulation of Thermal Behavior for Networks-on-Chip
Tim Wegner et al, University of Rostock (DE)

Traffic Characterization for Multicasting in NoC
V. Laxmi et al, National Institute of Technology (IN)

SoC Chip Scheduler Embodying I-SLIP Algorithm
Trupti B. Salankar et al, NAGPUR

Layered Spiral Algorithm for Memory-Aware Mapping and Scheduling on Network-on-Chip
Shuo Li et al, Royal Institute of Technology (SE)

Implementation Exploration for a Self Reconfigurable Interconnection Network in DRRA
Muhammad Shami et al, Royal Inst. of Technology (SE)

High-Performance NoC Interface with Interrupt Batching for Micronmesh MPSoC Prototype Platform on FPGA
Heikki Kariniemi et al, Tampere Univ. of Technology (FI)

NoC-based CSP Support for a Java Chip Multiprocessor
Flavius Gruian et al, Lund University (SE)

Calibration of Sigma Delta Analog-to-Digital Converters Based on Histogram Test Methods
Armin Jalili et al, Isfahan University of Technology (IR)

A Second-Order Low-Power $\Delta\sum$ Modulator For Pressure Sensor Applications
Tero Nieminen et al, Aalto University (FI)

A 500-MHz Low-Voltage Programmable Gain Amplifier for HD Video in 65-nm CMOS
Syed Ahmed Aamir et al, Linköping University (SE)

A novel transimpedance amplifier with variable gain
Pietro Monsurrò et al, Università di Roma (IT)

Diode Based Charge Pump Design using 0.35µm Technology
Muahammad Adeel Ansari et al, Royal Institute of Technology (SE)

An 8-bit 156nw 11.25 kS/s 0.18um two-Step-SAR for RFID applications Using Novel DAC Architecture
Iman Kianpour et al, Sabzevar Tarbiat Moallem University (IR)

Digital PVT Calibration of a Frequency-to-Voltage Converter
Jørgen Andreas Michaelsen et al, University of Oslo (NO)

7.1 RECEIVERS AND TRANSMITTERS

CHAIR: DAG WISLAND, NOVELDA (NO)

11.10 A 175µW 100MHz-2GHz inductorless receiver front-end in 65nm CMOS
Carl Bryant et al, Lund University (SE)

11.30 Higher order FFSFR coupled micromechanical mixer-filters integrated in CMOS
Jan Erik Ramstad et al, University of Oslo (NO)

11.50 A 9.2pJ/pulse UWB-IR Transmitter with Tunable Amplitude for Wireless Sensor Tags in 0.18um CMOS
David Sarmiento Mendoza et al, Royal Institute of Technology (SE)

7.2 DEPENDABILITY AND TESTING

CHAIR: PEETER ELLERVEE, TALLINN UNIV. OF TECHNOLOGY (EE)

11.10 High-Level Design Error Diagnosis Using Backtrace on Decision Diagrams
Jaan Raik et al, Tallinn Univ. of Technology (EE)

11.30 Generic Partial Dynamic Reconfiguration Controller for Fault Tolerant Designs Based on FPGA
Martin Straka et al, Brno Univ. of Techn. (CZ)

11.50 SfW Method: Delay Test Generation for Simple Chain Wrapper Architecture
Marcel Balaz, Slovak Academy of Sciences (SK)

12.10 Lunch

13.10 **Invited talk: Mixed-Signal versus Purely-Digital Self-Calibration of High-Resolution Pipeline A/D Converters**
Joao Goes, Universidade Nova de Lisboa (PT)

8.1 A/D -CONVERTERS

CHAIR: TOR S. LANDE, OSLO UNIVERSITY (NO)

13.55 On CMOS Scaling and A/D-Converter Performance
Bengt E. Jonsson, ADMS Design AB (SE)

14.15 An 1.2V 440-MS/s 0.13-um CMOS Pipelined Analog-to-Digital Converter With 5-8bit Mode Selection
Tero Nieminen, Aalto University (FI)

14.35 A 290uA, 3.2 MHz 4-bit Phase ADC for Constant Envelope, Ultra-low Power Radio
Budhaditya Banerjee et al, CSEM (CH)

14.55 Design of CMOS Sampling Switch for Ultra-Low Power ADCs in Biomedical Applications
Dai Zhang et al, Linköping University (SE)

8.2 NETWORK-ON-CHIP

CHAIR: JARI NURMI, TAMPERE UNIV. OF TECHNOLOGY

13.55 Energy Aware Design Methodologies for Application Specific NoC
Naveen Choudhary et al, Malaviya National Institute of Technology (IN)

14.15 A Scalable, Non-Interfering, Synthesizable Network-on-Chip Monitor
Antti ALHONEN et al, Tampere University of Technology (FI)

14.35 An Efficient VFI-Based NoC Architecture Using Johnson-Encoded Reconfigurable FIFOs

Amir-Mohammad Rahmani et al, University of Turku (FI)

14.55 A Hybrid NoC Combining SDM-Based Circuit Switching with Packet Switching for Real-Time Applications
Angelo Kuti Lusala et al, UC Louvain (BE)

15.15 Closing remarks and NORCHIP 2011

SESSION ORGANISATION

Both oral and poster presentations have been carefully selected through a regular review process and they will all appear in the proceedings. Equal quality measures have been applied to posters and lectures. Papers for oral presentation are selected based on thematic composition of sessions.

PROCEEDINGS

USB stick proceedings of the conference contributions will be distributed upon registration. Each participant will receive a copy of the proceedings. Proceedings and all presentations will be in English.

BEST ANALOG PAPERS

The Management Committee has since 1992 made special issues of the Springer International *Journal on Analog Integrated Circuits and Signal Processing*. Also this year we will publish a number of the best analog papers in the journal.
http://www.springer.com/engineering/circuits+%26+systems/journal/10470

BEST DIGITAL PAPERS

The best digital papers will be invited to publish in the international Elsevier journal *Embedded Hardware Design (MICPRO)*.
http://www.elsevier.com/wps/find/journaldescription.cws_home/525449/description#description

GENERAL SCOPE OF THE CONFERENCE

The NORCHIP conference is the main microelectronics event of the Nordic countries. The annual IEEE CAS sponsored conference covers all areas of microelectronics, spanning from large digital systems to simple analog circuits. The wide scope of NORCHIP is intentional promoting cross-field collaboration. NORCHIP is a well established conference with representation from both academia and industry. Papers of the highest scientific and technical quality are presented together with selected invited speakers and pre-conference tutorial sessions.

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- Kari Halonen, Helsinki Univ. of Technology (FI)
- Jan Madsen, Technical University of Denmark (DK)
- Viktor Öwall, Lund University (SE)
- Jari Nurmi, Tampere University of Technology (FI)
- Peeter Ellervee, Tallinn Univ. of Technology (EE)

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All submitted contributions have been reviewed by the following Committee:

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- Chairman: Ivan Ring Nielsen, Technoconsult (DK)
- Jari Nurmi, Tampere University of Technology (FI)

CONFERENCE VENUE / ACCOMMODATION

The conference location is in the heart of Tampere at:

Scandic Tampere City
Hämeenkatu 1
FI-33100 Tampere
Finland
http://www.scandichotels.com/Hotels/Countries/Finland/Tampere/Hotels/Scandic-Tampere-City/
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REGISTRATION

The enclosed registration form must be completed and returned to the Conference Secretariat, together with full payment. The registration fee of EUR 430 includes proceedings, banquette dinner, lunches and coffee breaks. The fee for the tutorial is charged separately. Registration deadline is *2 November*. Registrations are acknowledged upon reception.

PRE-CONFERENCE TUTORIAL

A tutorial on Hardware/Software Codesign of Embedded Systems using GEZEL is organized on 14 November. Further info on www.norchip.org.