

29th Norchip Conference

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DSP Architecture Optimization

Abstract

DSP architecture design has to tightly couple algorithmic and technology parameters in order to maximize system energy efficiency. Traditionally, DSP algorithms and their chip architectures are developed by different engineering teams, resulting in suboptimal designs. The ability to quickly explore many architectural realizations is essential for selecting the architecture that best utilizes the intrinsic computational efficiency of silicon technology. At the same time, more flexibility to support multiple operation modes and/or standards is needed.

This tutorial presents a methodology for algorithm-architecture-circuit co-design that leads to a hardware implementation optimized for performance, power, and area. The methodology is based on a high-level data flow graph (DFG) design model and several optimization routines to create many different architectural solutions, within constraints dictated by the underlying technology. Once architectural solutions are available, any of the architecture design points can be mapped through commercial and semi-custom flows to field-programmable gate array (FPGA) and application-specific integrated circuit (ASIC) hardware platforms. As a final step, FPGA-based logic analysis is used to verify ASIC chips using the same design environment.

The methodology has been applied to diverse range of applications, which span about 4 orders of magnitude in sampling speed and 3 orders of magnitude in power density. As an example of leakage-limited design, neural-spike processors for brain-machine interface (BMI) applications will be discussed, followed by an outlook and concluding remarks.

Outline:

- 13:00 Introduction to DSP architecture optimization
- 13:30 Circuit optimization
- 14:15 Architecture flexibility
- 15:00 Coffee break
- 15:20 Simulink-hardware flow
- 16:00 Design example: kHz-rate neural processors
- 16:45 Summary and conclusions

References:

D. Marković and R.W. Brodersen, "DSP Architecture Design Essentials," Springer 2011 (to appear)

Dejan Marković is an Assistant Professor of Electrical Engineering at the University of California, Los Angeles. He completed the Ph.D. degree in 2006 at the University of California, Berkeley. In recognition of the impact of his Ph.D. work, he was awarded 2007 David J. Sakrison Memorial Prize at UC Berkeley. His current research is focused on integrated circuits for emerging radio and healthcare systems, programmable ICs, design with post-CMOS devices, optimization methods and CAD flows. He received an NSF CAREER Award in 2009. In 2010, he was a co-recipient of ISSCC Jack Raper Award for Outstanding Technology Directions and a winner of the DAC/ISSCC Student Design Contest.

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